**PATENT**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant No. | : | 10/662,391 |
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| Applicant | : | James BREISCH et al. |
| Filed | : | September 16, 2003 |
| For | : | DUAL REFERENCED MICROSTRIP |
| Group Art Unit | : | 2815 |
| Examiner | : | Jesse A. FENTY |

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M/S: AMENDMENT
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CERTIFICATION OF FACSIMILE TRANSMISSION
I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office, Fax No. (571) 273-8300, on October 14, 2005.

Thea Wagner

**RESPONSE TO OFFICE ACTION**

Sir:

In response to the Final Office Action dated June 14, 2005, the time for response having been extended by petition and payment of fees to October 14, 2005, please amend the above-identified application as follows:

**Amendments to the Claims** begin on page 2 of this paper.

**Remarks/Arguments** begin on page 5 of this paper.

# DUAL REFERENCED MICROSTRIP

[0001] This application is a continuation of U.S. Patent Application Serial No. 10/060,363, filed February 1, 2002, now United States Patent Number 6,686,819 and incorporated herein by reference in its entirety.

## FIELD OF THE INVENTION

[0002] The invention relates dual referenced microstrip structures for signal propagation in packages having semiconductor circuits.

## BACKGROUND

[0003] As the speed of signals flowing between a packaged device and a printed circuit board to which it is coupled increases, the need to reduce signal discontinuities caused by changes in impedance between the package and the printed circuit board increases. Minimization of discontinuities allows for high bandwidth and high signal quality. Discontinuities include changes in impedance of a transmission line and/or signal reference of a transmission line over which a signal is traveling.

[0004] To ensure proper operation between various chips on a printed circuit board, manufacturers specify the characteristic impedance of signal paths running on or within the printed circuit board. Manufacturers also provide a tolerance for the characteristic impedance of these traces. For example, the characteristic impedance of system bus trace may be specified as being 50 Ohms ± 15 %.

[0005] Various design guidelines have been developed to maintain trace impedance within specified tolerance on the printed circuit board. These guidelines are, by their nature, restrictive. One such guideline is the "Intel ® Pentium ® 4 Processor in 478-pin Package and Intel ® 845 Chipset Platform Design Guide," which may be found at the Intel ® Developer Web Site at http://developer.intel.com/design/chipsets/designex/29835401.pdf. The Intel ® guideline describes a four layer printed circuit board design that includes two external signal layers (one each on a primary and secondary side, respectively) and two internal planes. One of the internal